50 Gbits/sec: The Next Mainstream Wireline Interconnect Lane Bit Rate

Forum 4: Emerging Short-Reach and High-Density Interconnect Solutions for Internet of Everything

Chris Cole

Thé Linh Nguyen

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FINISAR®

Outline

- **Wireline Overview**
- 10 Gb/s Lane Optical Interfaces
- 25 Gb/s Lane Optical Interfaces
- 50 Gb/s Modulation Selection
- 50 Gb/s Lane Optical Interfaces
- Laser Driver IC
- Trans-Impedance Amplifier IC
- Clock Data Recovery IC
- ADC/DSP IC
- Summary
- References

Major Applications

- Ethernet (Datacom)
  - IEEE 802.3 standards
  - Mainstream High-volume Interfaces
- Transport Clients (Telecom)
  - ITU-T standards
  - Variants of Ethernet interfaces
- FibreChannel
  - T11 standards
  - Storage
- InfiniBand
  - Low latency is key requirement (ex. no FEC)
  - HPC (High Performance Computing)

Ethernet Data Rates (≥10 Gb/s)

- Ethernet data rate is set by the rate of the MAC (Media Access Controller)
- Existing Ethernet data rate progression (Gb/s):

  10 → 40 → 100
- Rates in standardization by IEEE 802.3:
  - 25 Gb/s (nearly completed)
  - 50 Gb/s (just started)
  - 200 Gb/s (just started)
  - 400 Gb/s
- Resulting Ethernet data rate progression (Gb/s):

  10 → 25 → 50 *(& 40)* → 100 → 200 → 400

Lane Rates & Technology (≥10 Gb/s)

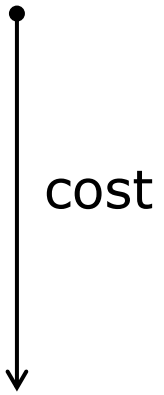
- In volume use
  - 10 Gb/s: 10Gbaud NRZ w/o FEC
  - 25 Gb/s: 25Gbaud NRZ w/o & w/ FEC
- In development for near-term volume use
  - 50 Gb/s: 25Gbaud PAM4 w/ FEC [1]
- In development for near-term specialty apps.
  - 50 Gb/s: 50GBaud NRZ w/o FEC [2]
- In development for long-term use
  - 100 Gb/s: 50GBaud PAM4 w/ FEC [2]
  - 100 Gb/s: Complex Mod., ex. DMT, w/ FEC [2]

[1] Presentation focus

[2] Not discussed in this presentation

Ethernet Optics Designations & Reach

- SRn: ≤ 100m to 300m MMF (& SWDMn)
- DRn: ≤ 500m SMF (& PSMn)
- FRn: ≤ 2km SMF (& CWDMn)
- LRn: ≤ 10km SMF
- ERn: ≤ 40km SMF



- "n" designates number of lanes, either parallel fiber pairs or duplex wavelengths
- MMF: Multi-Mode Fiber, for lowest cost lasers
- SMF: Single-Mode Fiber, for longer reaches
- LC: Lucent Connector, duplex (2x) connector
- MPO: Multi-fiber Push-On, parallel connector

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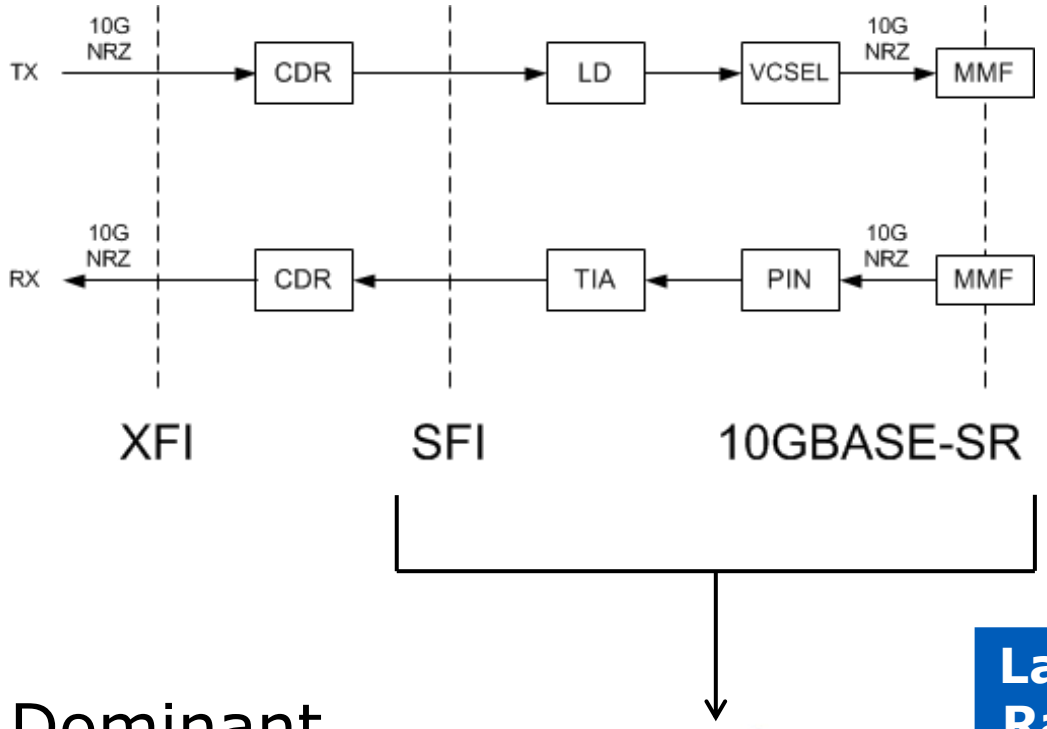
10GBASE-SR 850nm MMF Optics



Optics ICs:

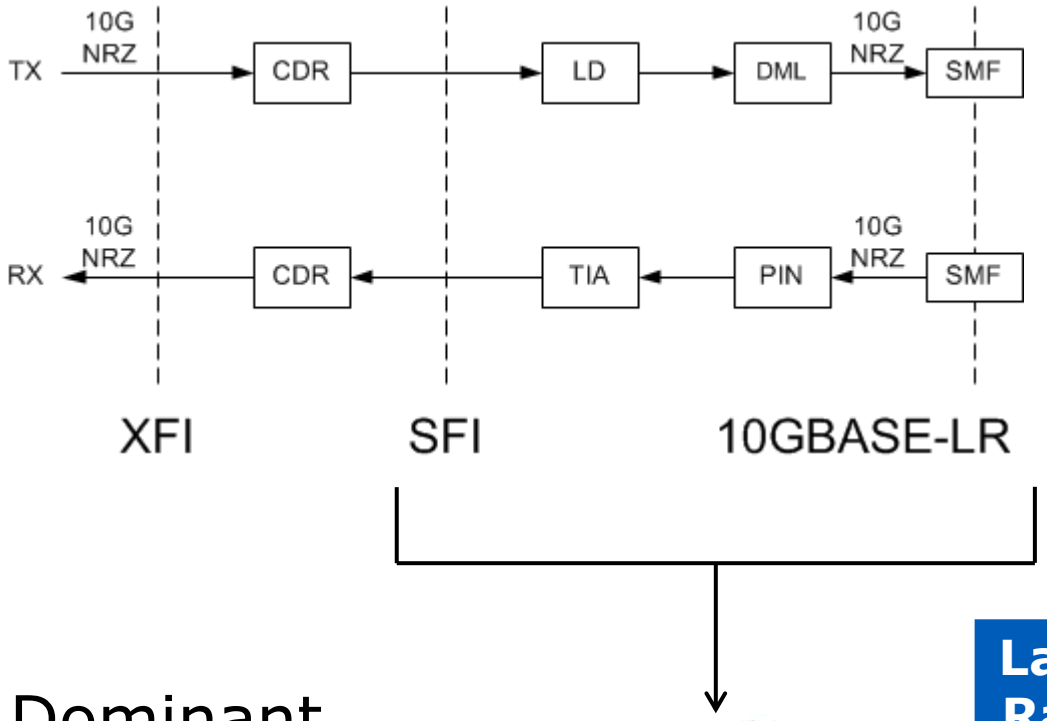
- LD: Laser Driver
- TIA: Trans-Impedance Amp
- CDR: Clock Data Recovery

(optics defined on next page)

Dominant, standard form factor: SFP+ w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
10	1	1	10

10GBASE-LR 1310nm SMF Optics



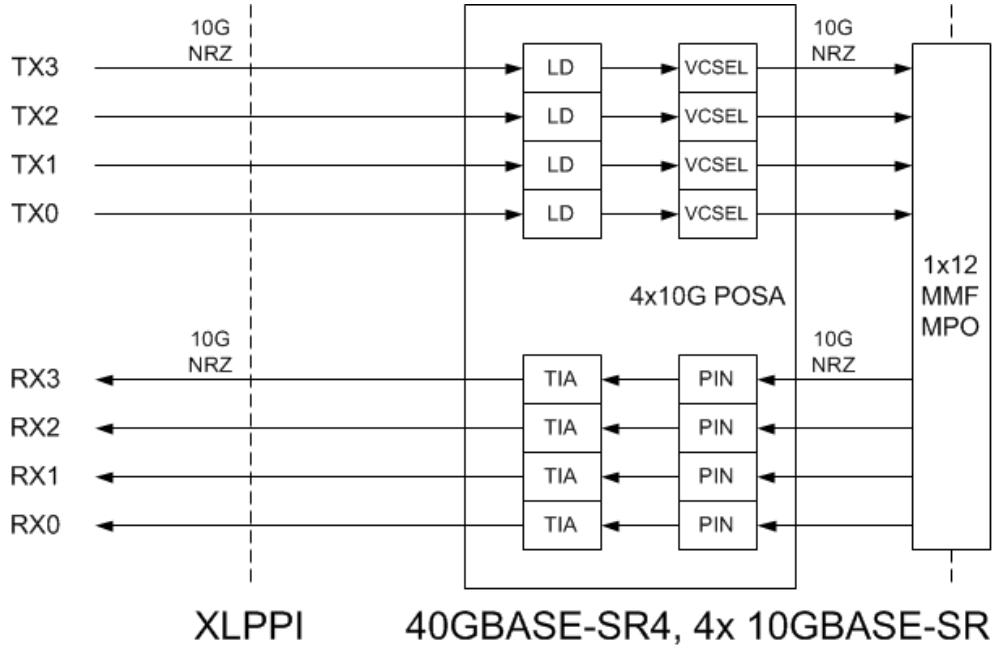
Optics:

- VCSEL: Vertical Cavity Surface Emitting Laser
- DML: Directly Modulated Laser
- PIN: p-type | intrinsic | n-type (photodiode)

Dominant, standard form factor: SFP+ w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
10	1	1	10

40GBASE-SR4 850nm MMF Optics

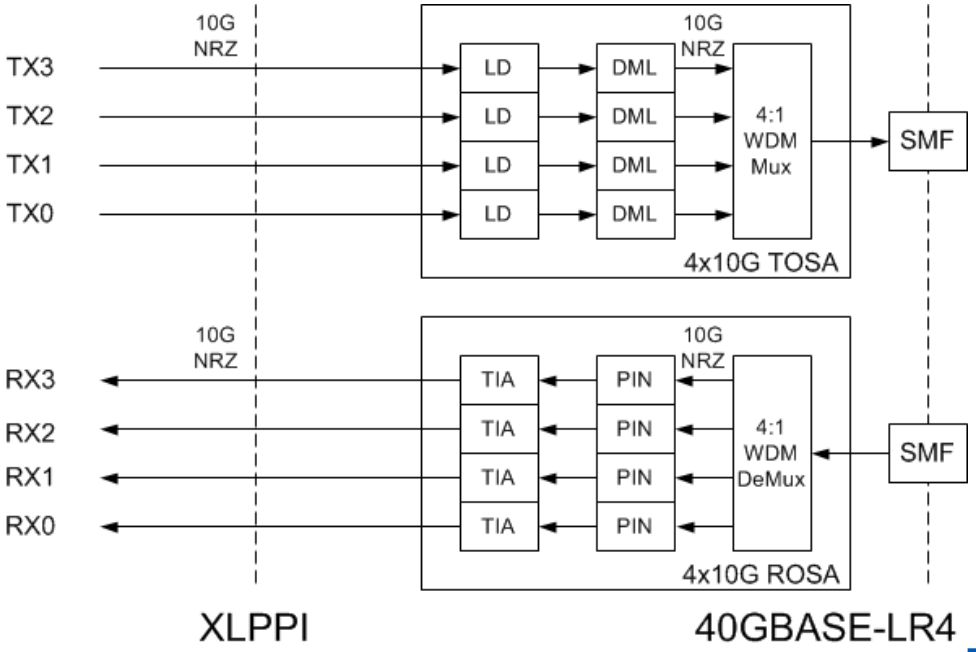


40G PSM4 is Parallel SMF version

Dominant, standard form factor: QSFP+ w/ MPO

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
10	4	1	40

40GBASE-LR4 1310nm SMF Optics



40G SWDM4 is WDM MMF version

Dominant, standard form factor: QSFP+ w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
10	1	4	40

10 Gb/s Lane Optical Interfaces

Lane Rate	No. of Lanes		Data Rate	SW code	LW code
Gb/s	fiber pairs	λ	Gb/s	(MMF)	(SMF)
10	1	1	10	**SR**	**LR**
10	4	1	40	**SR4**	*PSM4*
10	1	4	40	*SWDM4*	**LR4**
10	10	1	100	**SR10**	

IEEE standards in BOLD; MSA or proprietary in *ITALICS*

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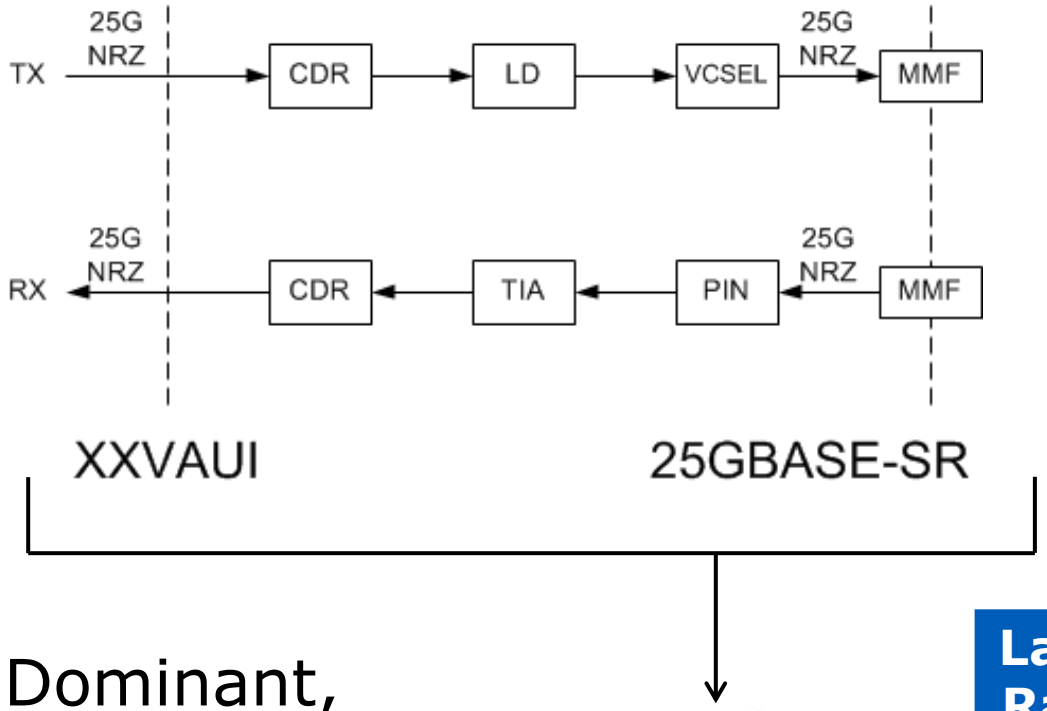
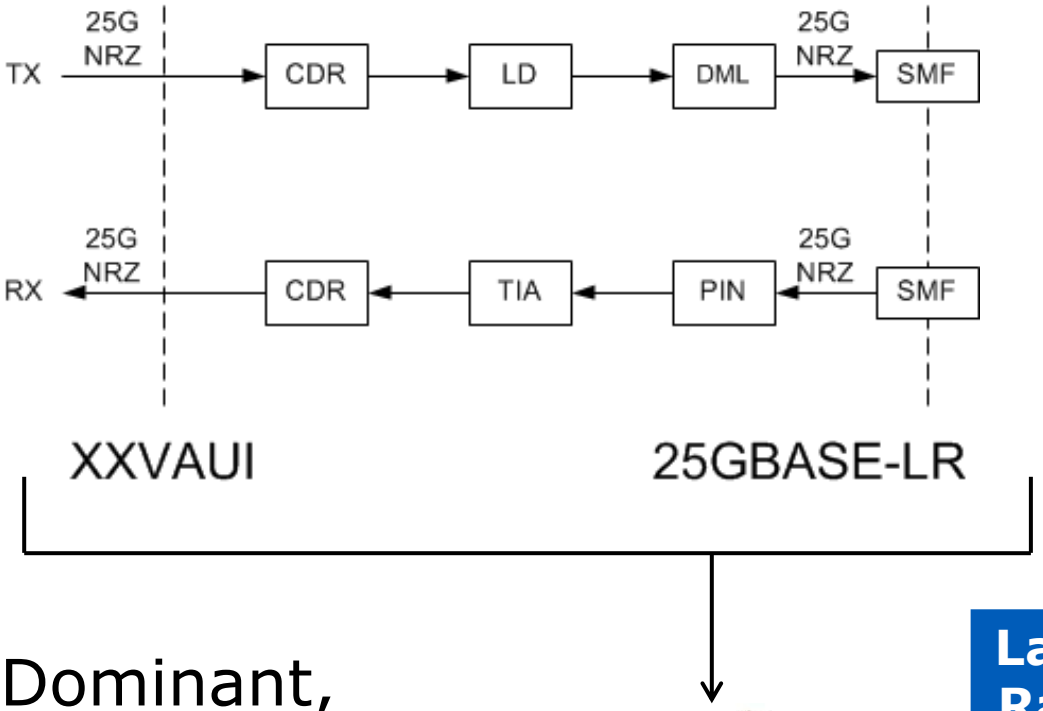
25GBASE-SR 850nm MMF Optics



Dominant, standard form factor: SFP28 w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
25	1	1	25

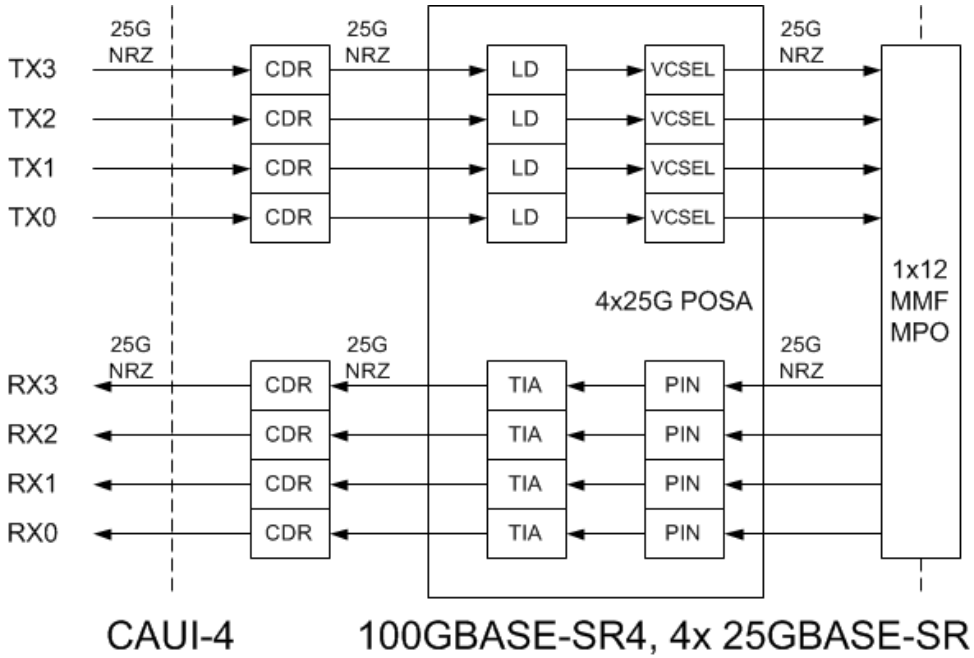
25GBASE-LR 1310nm SMF Optics



Dominant, standard form factor: SFP28 w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
25	1	1	25

100GBASE-SR4 850nm MMF Optics

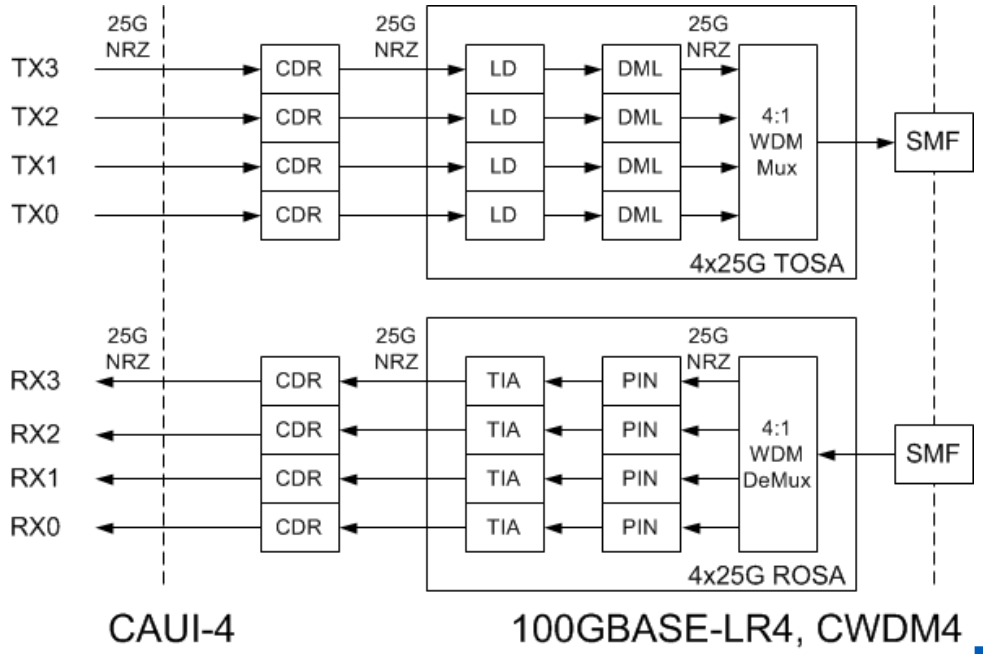


100G PSM4 is parallel SMF version

Dominant, standard form factor: QSFP28 w/ MPO

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
25	4	1	100

100GBASE-LR4 1310nm SMF Optics



100G SWDM4 is WDM MMF version

Dominant, standard form factor: QSFP28 w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
25	1	4	100

25 Gb/s Lane Optical Interfaces

Lane Rate	No. of Lanes		Data Rate	SW code	LW code
Gb/s	fiber pairs	λ	Gb/s	(MMF)	(SMF)
25	1	1	25	**SR**	**LR**
25	4	1	100	**SR4**	*PSM4*
25	1	4	100	*SWDM4*	**LR4**
25	8	1	200	SR8	*PSM8*
25	16	1	400	**SR16**	

IEEE standards in BOLD; MSA or proprietary in *ITALICS*

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Shannon-Hartley Theorem

$C = B \log_2 (1 + S/N)$

C ≜ Channel capacity

B ≜ Bandwidth

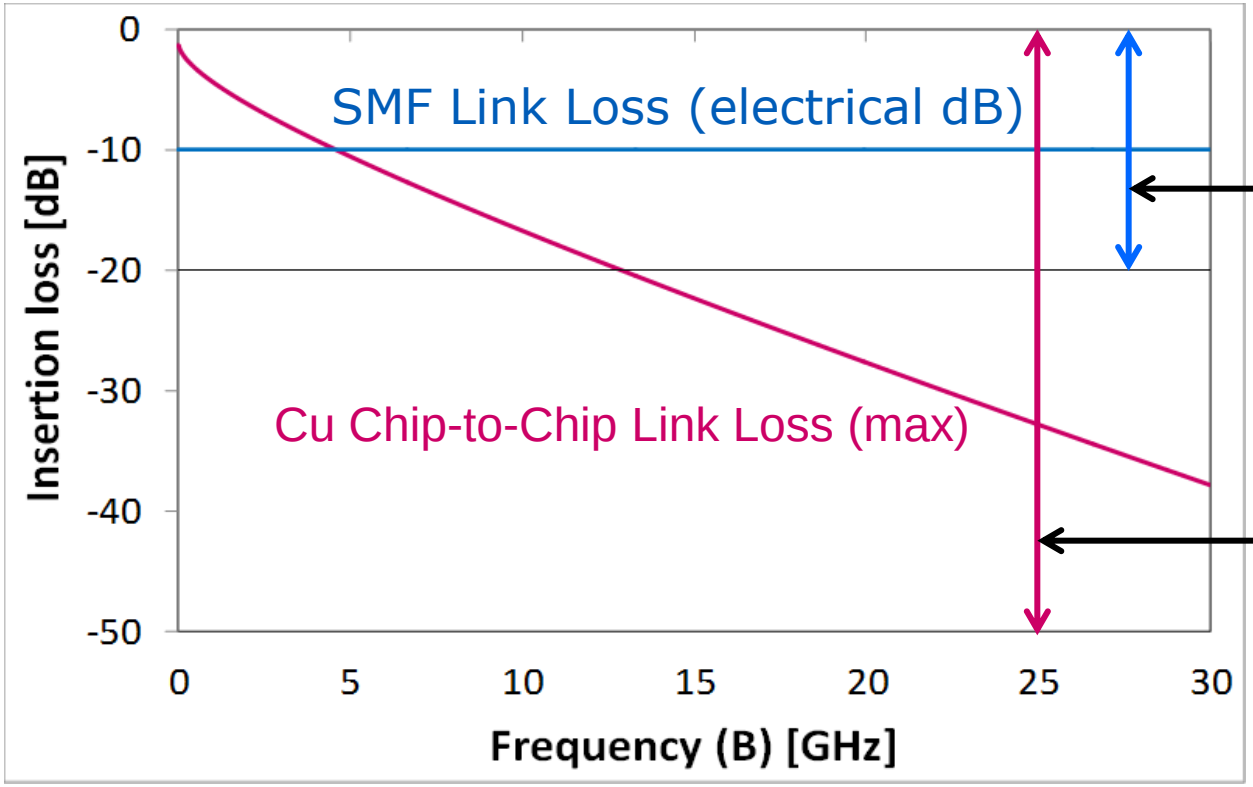
S ≜ Signal Power

N ≜ Noise Power

Guidance to increase C:

- If B limited, increase S/N to increase modulation order, i.e. more bits/Baud
- If S/N limited, increase B to increase Baud rate, i.e. switch faster

Cu vs. SMF Link Loss & TRX S/N



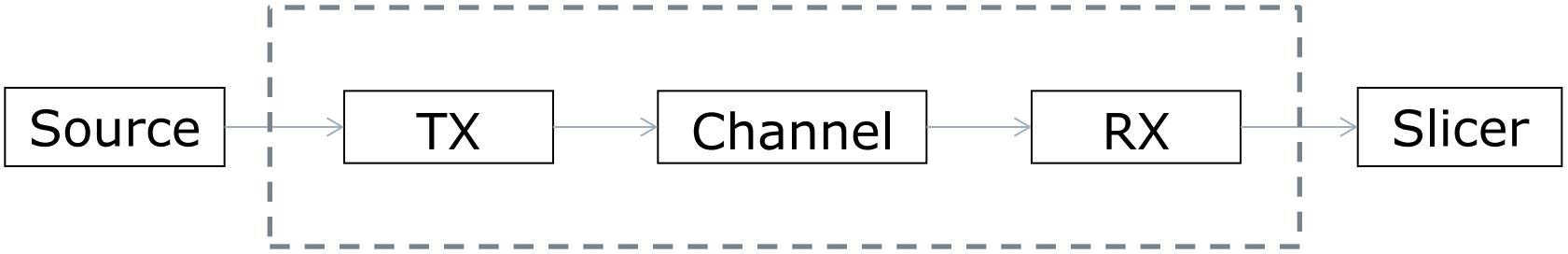
S/N (BTB) [dB][1] SMF TRX (DML TX, PIN RX, no FEC)

S/N (BTB) [dB][1] Cu TRX (ASIC SerDes, no FEC)

[1] electrical dB

- Cu channel limitation: Bandwidth (B)
- SMF channel limitation: S/N

Ideal SMF Link Model



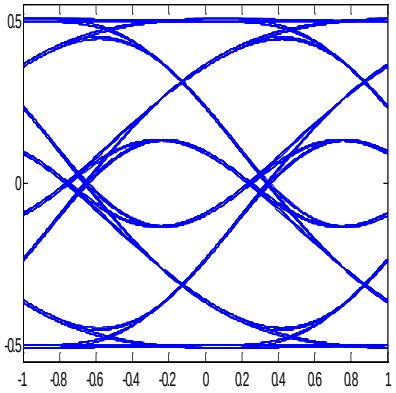
- SMF channel assumed ideal
- 4^{th} order BT filter model for TX $*$ Channel $*$ RX
- Bandwidth $\triangleq$ B = α * bit-rate
- Example bandwidths for bit rate = 56Gb/s
  - ex. 1: $\alpha = 0.25 \rightarrow$ B = 14GHz
  - ex. 2: $\alpha = 0.30 \rightarrow$ B = 17GHz

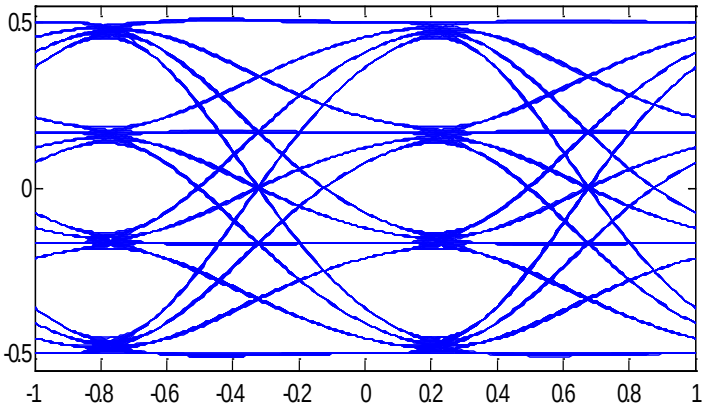
Slicer Input of Ideal SMF Link

NRZ

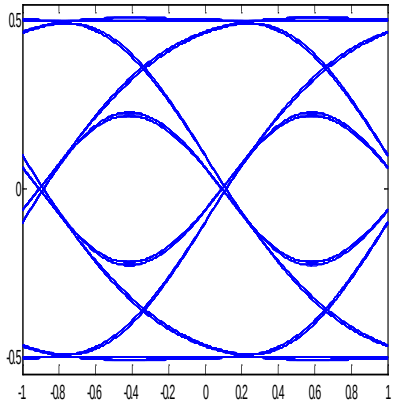
PAM4

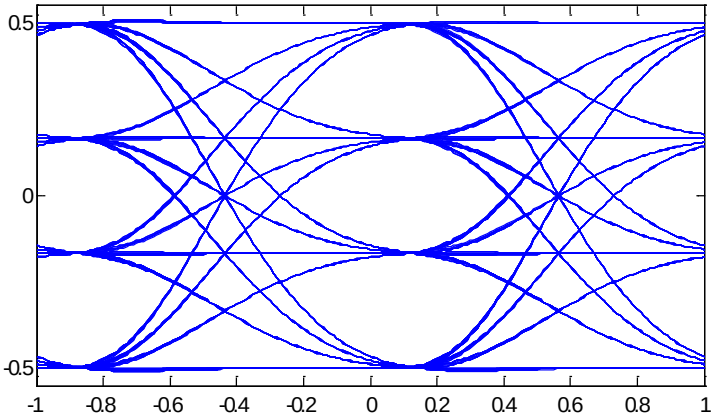
ex. 1
α = 0.25
(14 GHz)



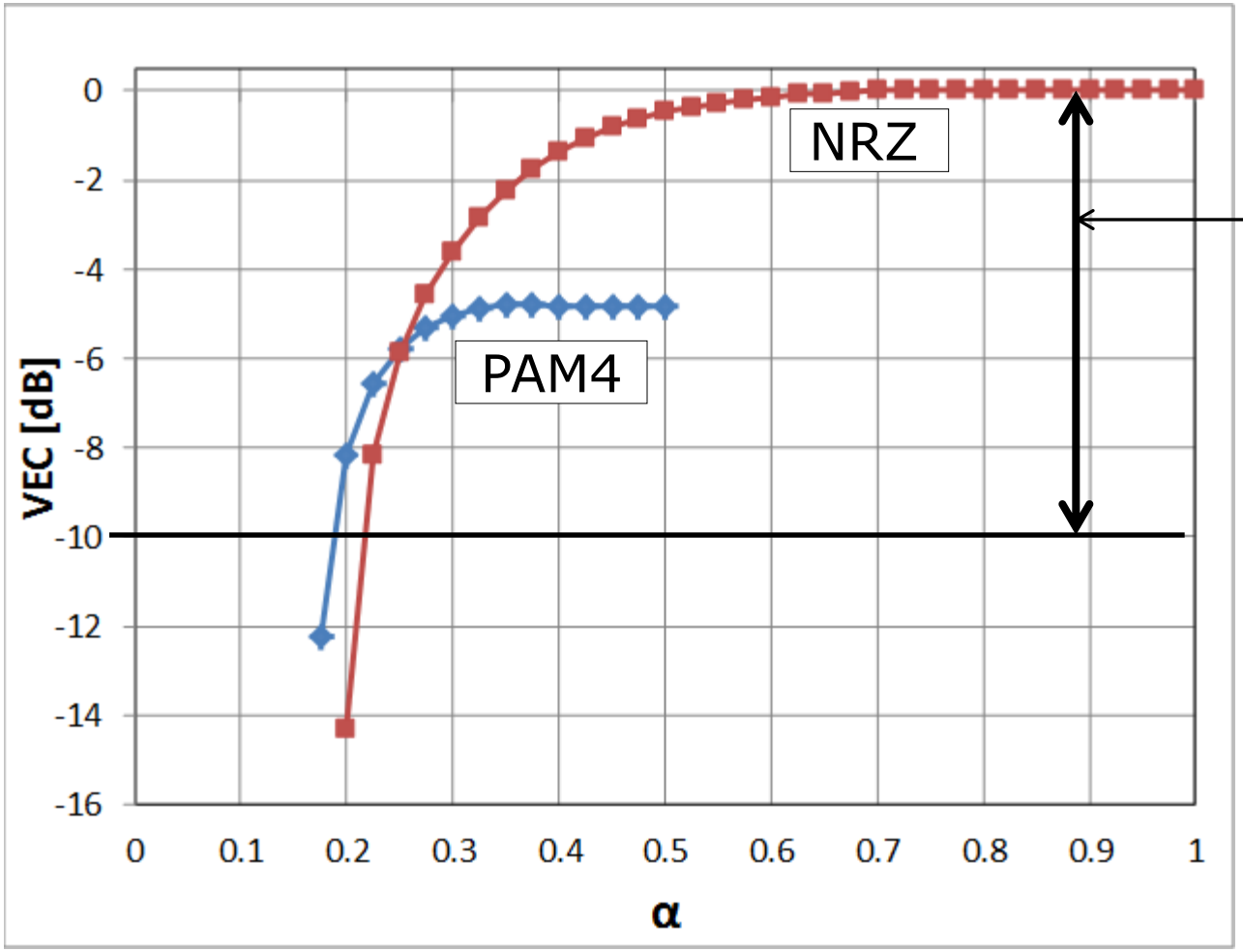


ex. 2
α = 0.30
(17 GHz)





Vertical Eye Closure at Slicer Input



S/N (BTB) [dB][1]
SMF TRX
(DML TX, PIN RX, no FEC)

[1] optical dB

50 Gb/s NRZ vs. PAM4 Optical Lanes

- 50G NRZ Advantages:
  - Optical SNR
  - Well understood development methodology ex. 10G NRZ → 25G NRZ
- 50G PAM4 Advantages:
  - 50G PAM4 IC ecosystem & volume
  - 25G NRZ optical packaging reuse
  - 25G NRZ SMF & MMF laser reuse
- Deciding factor in favor of 50G PAM4
  - Optics is the tail on the IC industry dog
  - PAM4 was developed for 50G ASIC SerDes because of channel bandwidth limitations
  - Despite SNR limitations optics tail wagged

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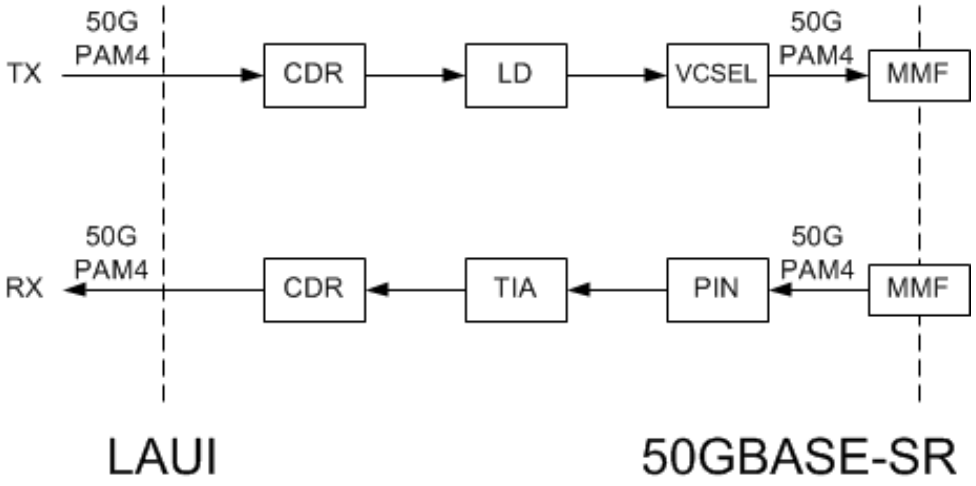
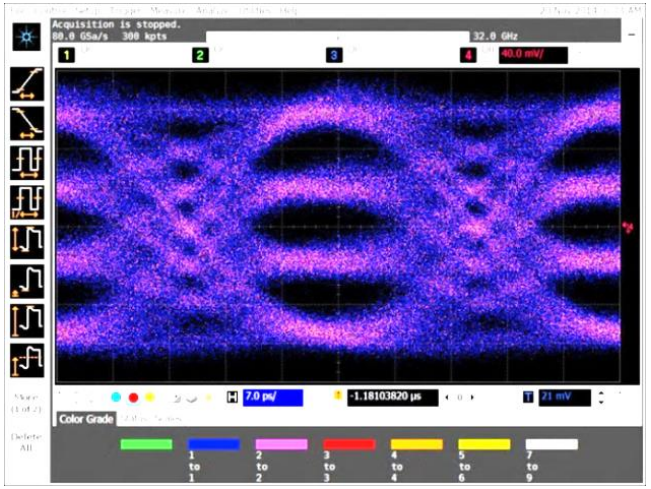


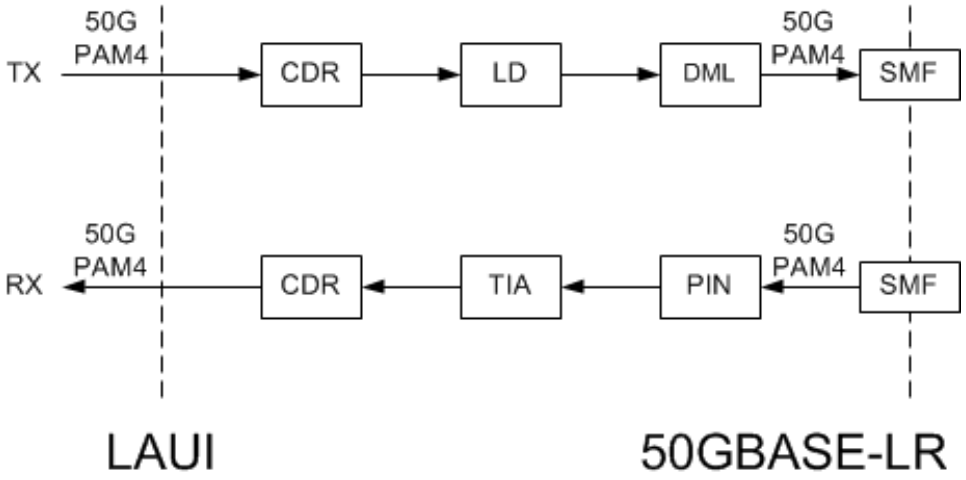
56Gb/s PAM4 optical eye



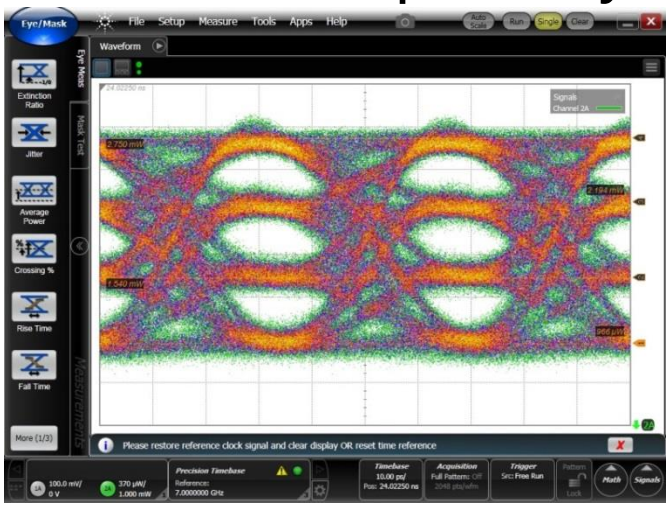
Likely dominant, standard form factor: SFP28 w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
50	1	1	50

50GBASE-LR 1310nm SMF Optics



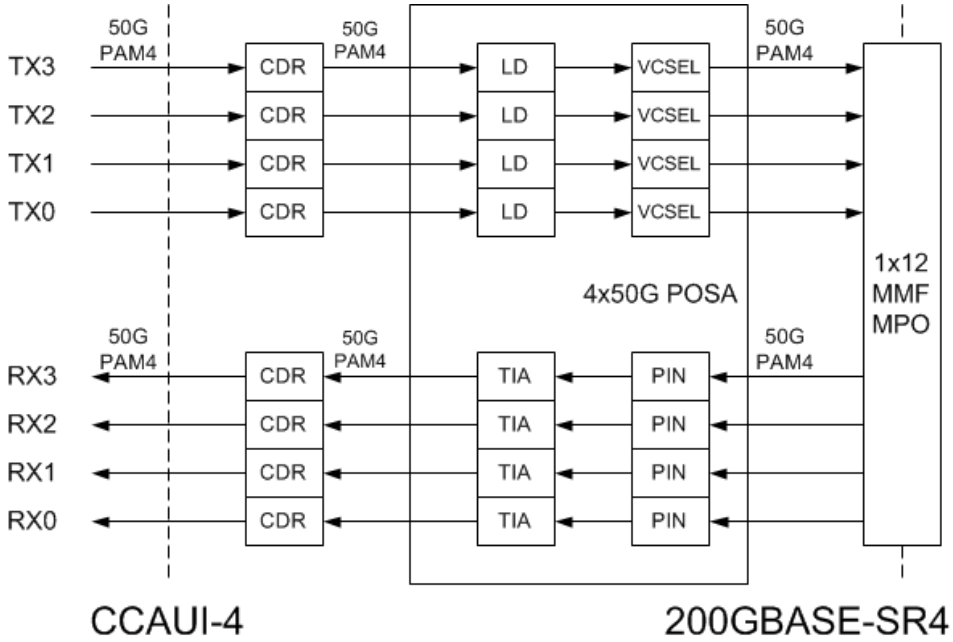
56Gb/s PAM4 optical eye



Likely dominant, standard form factor: SFP28 w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
50	1	1	50

200GBASE-SR4 850nm MMF Optics

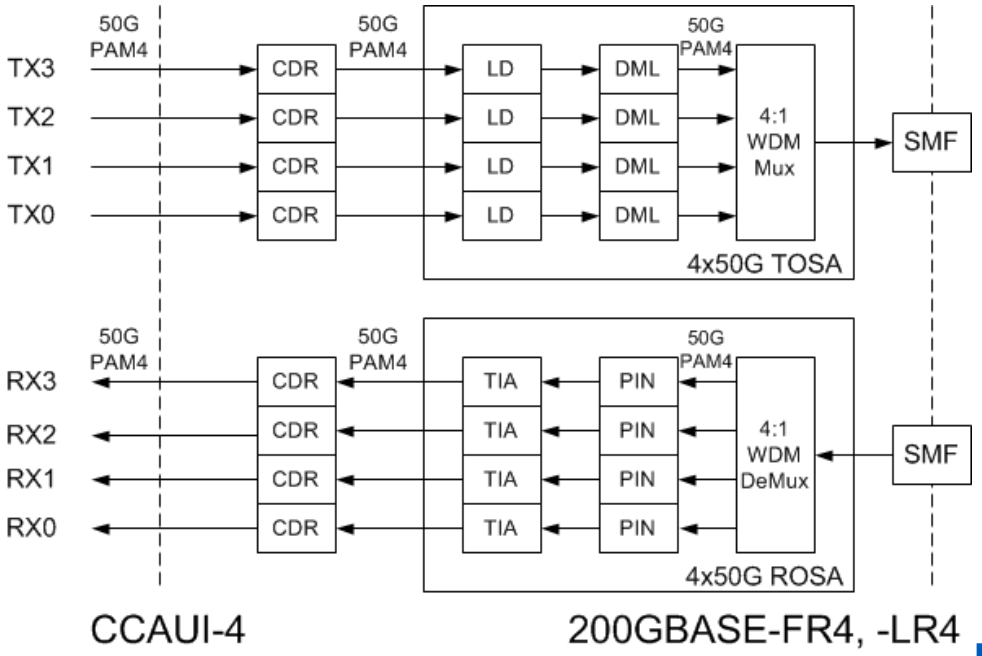


200G PSM4 is parallel SMF version

Likely dominant, standard form factor: QSFP28 w/ MPO

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
50	4	1	200

200GBASE-LR4 1310nm SMF Optics

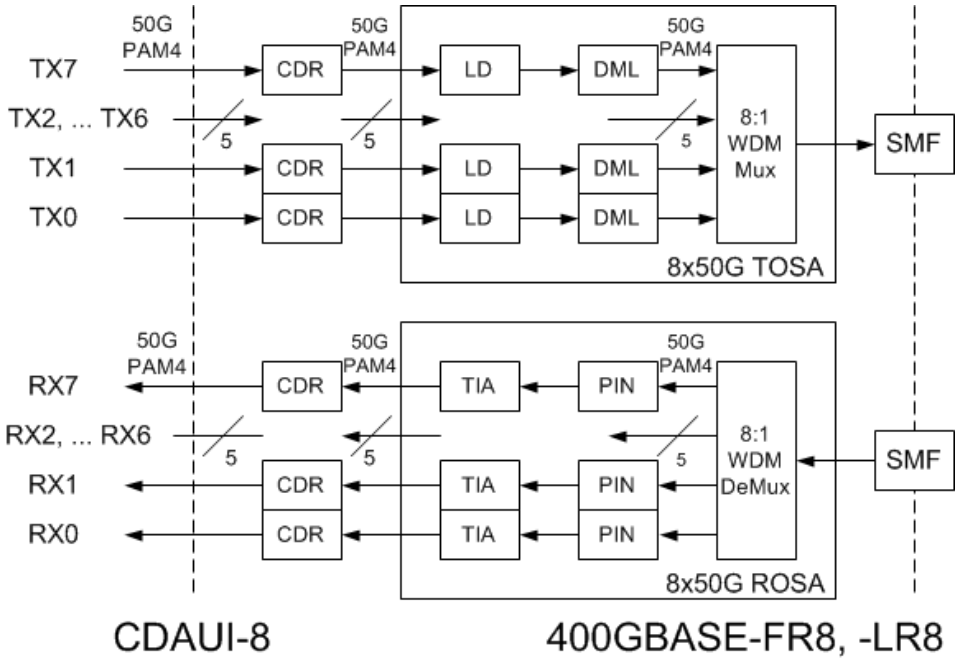


200G SWDM4 is WDM MMF version

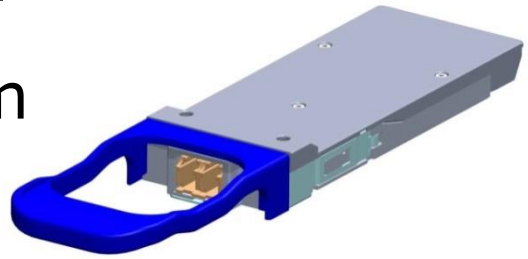
Likely dominant, standard form factor: QSFP28 w/ 2x LC

Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
50	1	4	200

400GBASE-LR8 1310nm SMF Optics



1st 400G SMF standard form factor: CFP8 w/ 2x LC



Lane Rate	No. of Lanes		Data Rate
Gb/s	fiber pairs	λ	Gb/s
50	1	8	400

50 Gb/s Lane Optical Interfaces

Lane Rate	No. of Lanes		Data Rate	SW code	LW code
Gb/s	fiber pairs	λ	Gb/s	(MMF)	(SMF)
50	1	1	50	SR	LR
50	1	2	100	*SWDM2*	LR2
50	4	1	200	SR4	*PSM4*
50	1	4	200	*SWDM4*	FR4, LR4
50	1	8	400		**FR8, LR8**

IEEE standards in BOLD; MSA or proprietary in *ITALICS*

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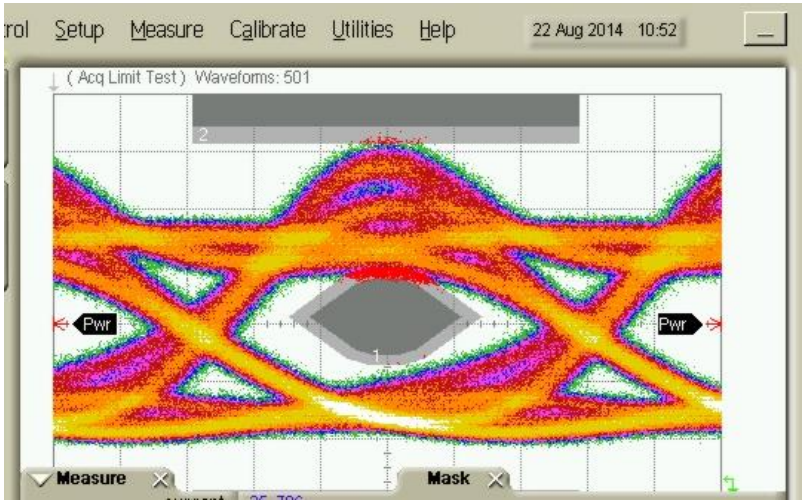
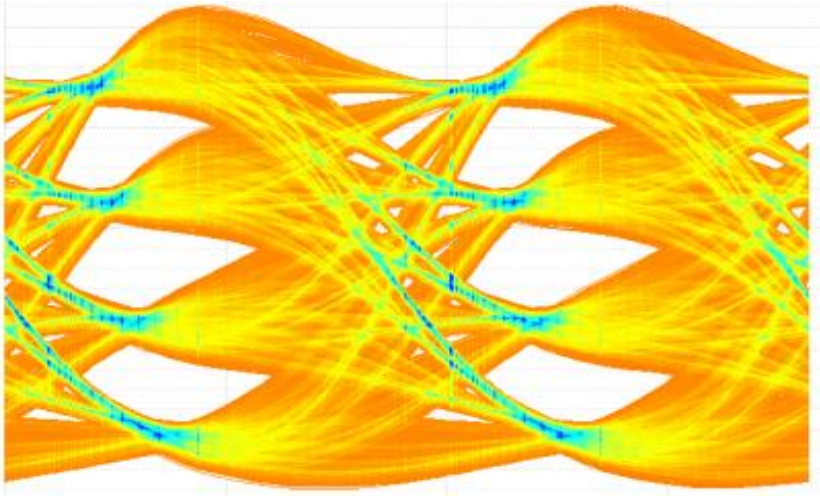
50 Gb/s PAM4 LD Requirements

- DML has different ON vs. OFF damping behavior
- More severe problem for PAM4 than NRZ

26 Gb/s NRZ optical DCA eye



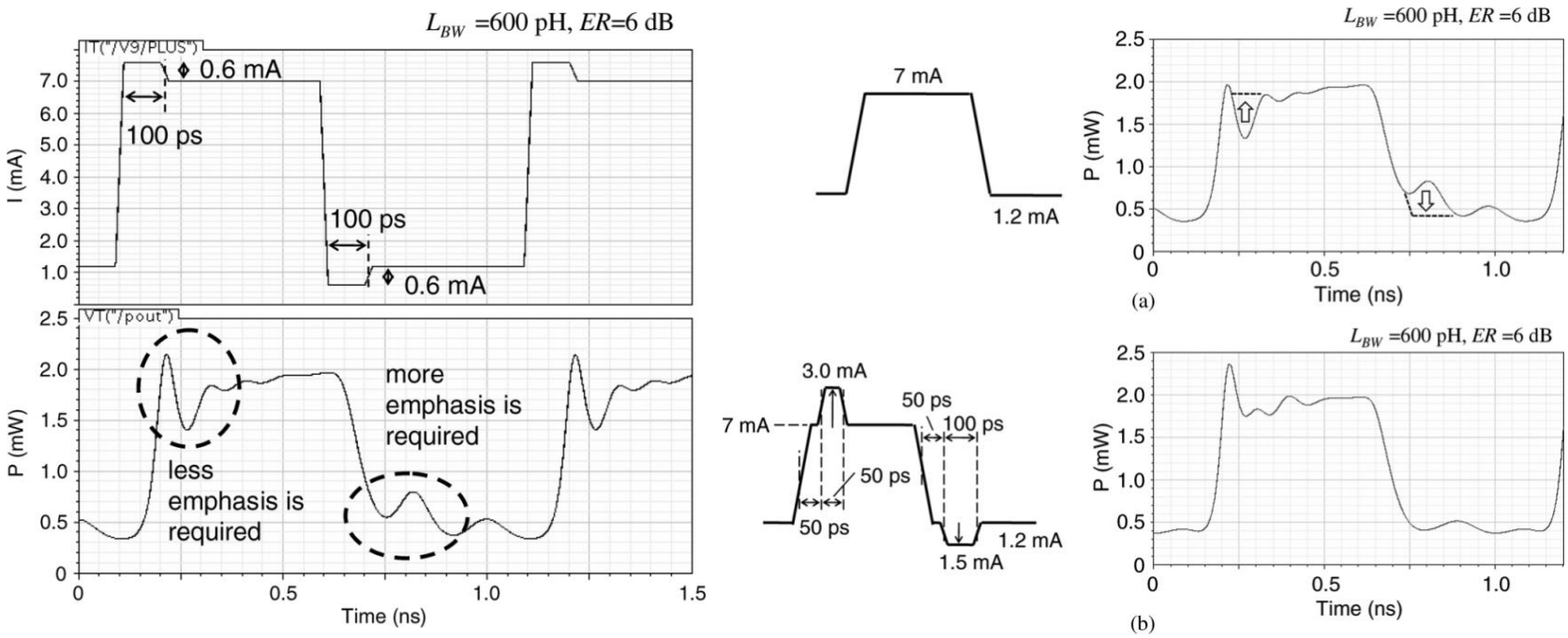
52 Gb/s PAM4 optical sim. eye



- Requires high-speed LD nonlinear compensation
- Requires linear transfer function LD to support multi-levels at similar low power as NRZ LD

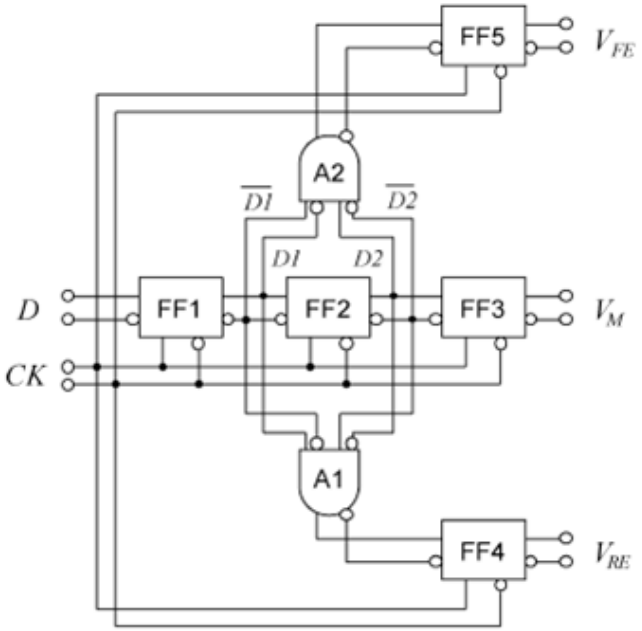
LD Nonlinear Pre-distortion

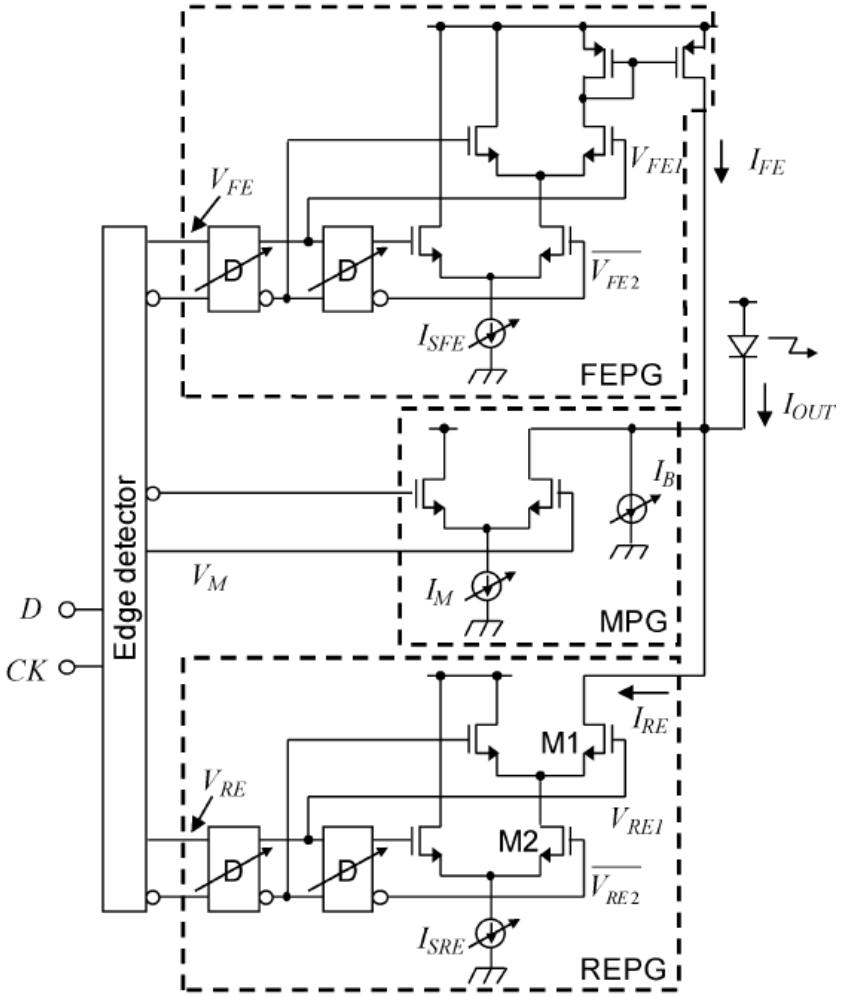
10 Gb/s LD nonlinear pre-distortion example [5]



LD Nonlinear Pre-distortion

Example edge detector circuit that distinguishes rising and falling edges to select different ON and OFF compensation

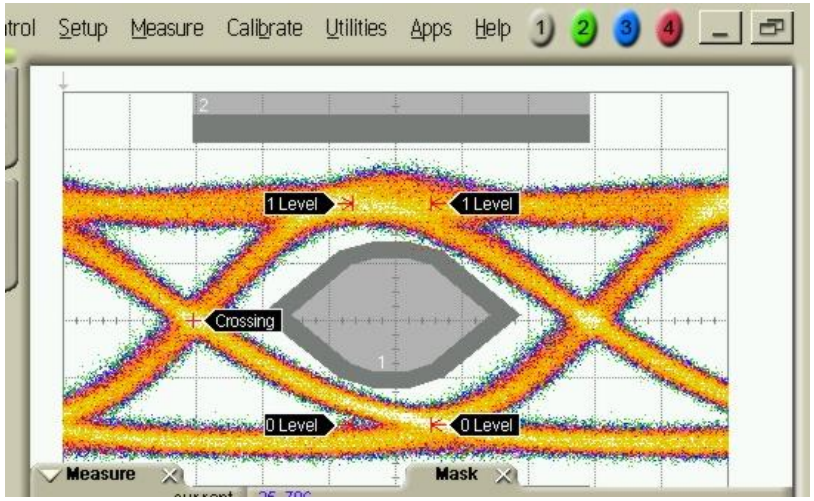




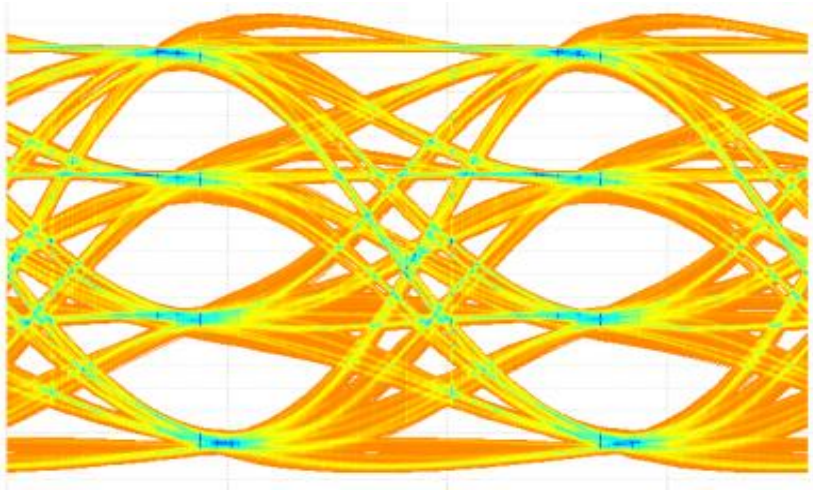
50 Gb/s PAM4 LD Example

- DML eyes using LD with nonlinear compensation followed by linear transfer function
- Enables use of existing 25G DMLs for PAM4

26 Gb/s NRZ optical DCA eye

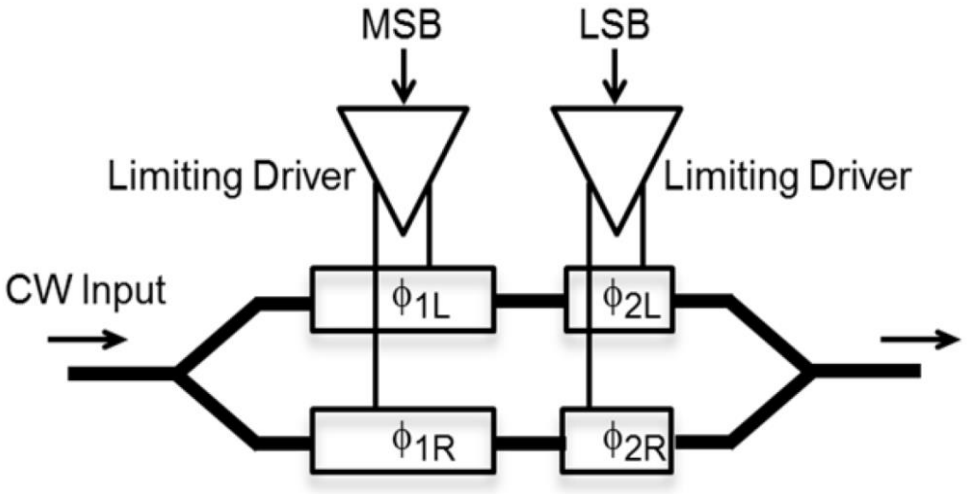


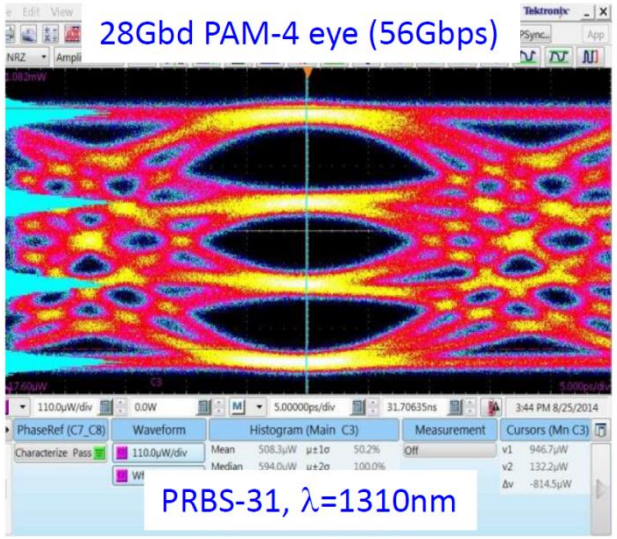
52 Gb/s PAM4 optical sim. eye



50 Gb/s PAM4 External Modulator

- DML alternative is Continuous Wave (CW) laser w/ linear Si Mach-Zehnder (MZ) modulator [2]
- Cascading binary weighted modulators, driven separately by NRZ bits, creates an optical DAC
- Ex. SiPIC with two NRZ modulator drivers [8]





- Major drawback is low output optical power

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- 50 Gb/s Modulation Selection
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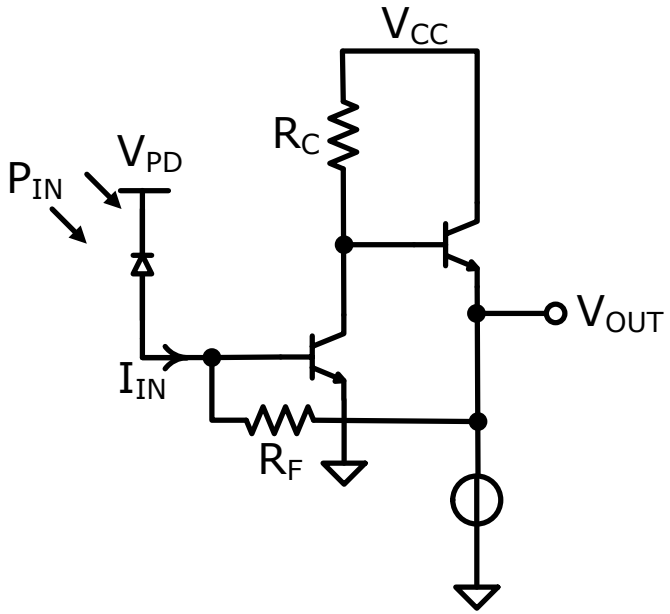
- Laser Driver IC
- **Trans-Impedance Amplifier IC**
- Clock Data Recovery IC
- ADC/DSP IC
- Summary
- References

50 Gb/s PAM4 TIA Requirements

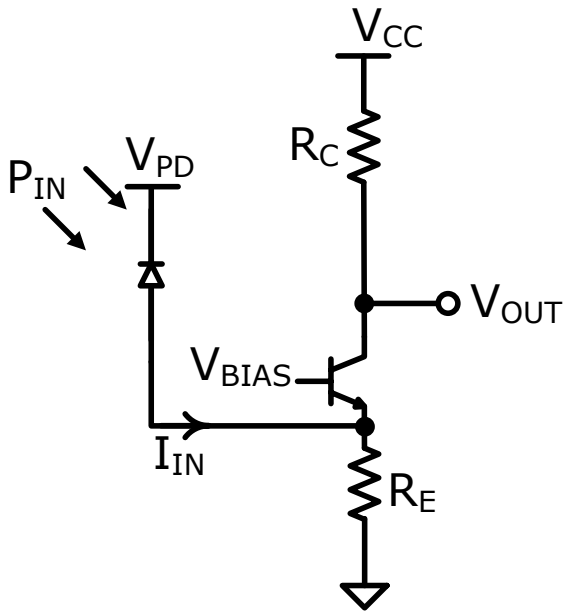
- 50G PAM4 OSNR ≈ 25G NRZ OSNR - 5dB
- 50G PAM4 RX_{sens} ≈ 25G NRZ Rx_{sens} - 5dB [4]
- Ex. requirements
  - 100GBASE-LR4 RX_{sens} = -10.6dBm OMA @1e-12 BER w/o FEC
  - 400GBASE-LR8 RX_{sens} = -15.1dBm OMA @2e-4 BER w/ KP4 FEC
- PAM4 receiver linearity requirement:
  - THD at Nyquist freq. < 4% over the full dynamic range
  - Requires higher open loop gain, so requires higher open loop bandwidth vs. NRZ

TIA Topologies

Shunt Feedback (SFB)



Common Base (CB)



TIA parameter	**SFB**	**CB**
Trans-impedance	$-R_f$	R_C
Input Impedance	$\frac{R_f}{1+g_m R_C}$	$\frac{1}{g_m}$

TIA Topologies Sensitivity Comparison

- Shunt Feedback (SFB)

$$\langle i_{in,Total}\rangle^2 = \frac{4kT}{R_f} + 4kTr_b\left(\frac{1}{R_f^2} + \omega^2 C_{PD}^2\right) + \frac{2qI_C}{g_m^2}\left(\frac{1}{R_f^2} + \omega^2 C_T^2\right) + \frac{4kT}{R_C}\left(\frac{1}{R_f^2} + \omega^2 C_T^2\right)$$

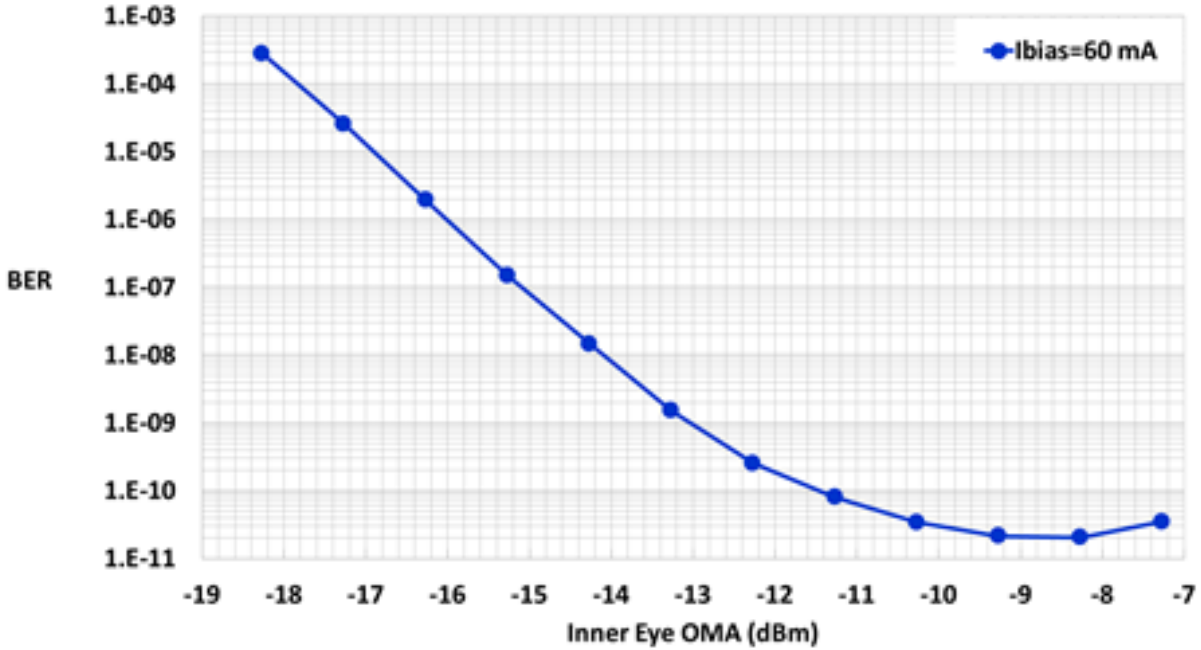
- Common Base (CB)

$$\langle i_{in,Total}\rangle^2 = \frac{4kT}{R_E} + 4kTr_b\left(\frac{1}{R_E^2} + \omega^2 C_{PD}^2\right) + \frac{2qI_C}{g_m^2}\left(\frac{1}{R_E^2} + \omega^2 C_T^2\right) + \frac{4kT}{R_C}\left(1 + \frac{\omega^2 C_T^2}{g_m^2}\right)$$

- Given a fixed V_{supply}, SFB operates at higher I_C than CB because it has no V drop across R_E
  - Higher I_C lowers transistor collector noise $2qI_C$, since it is being divided by g_m^2
  - Higher I_C enables larger transistor area reducing r_b without sacrificing f_T
- SFB RX_{sens} is ~1.5dB > CB, so better for PAM4

50 Gb/s PAM4 TIA Example

- 56 Gb/s DML TX source as shown on page 28
- RX_{sens} ≈ -17.5dBm OMA @ 2e-4 BER (KP4 FEC)
- Less margin than for 25 Gb/s NRZ optics
- Error floor makes FEC mandatory



Outline

- Wireline Overview
- 10 Gb/s Lane Optical Interfaces
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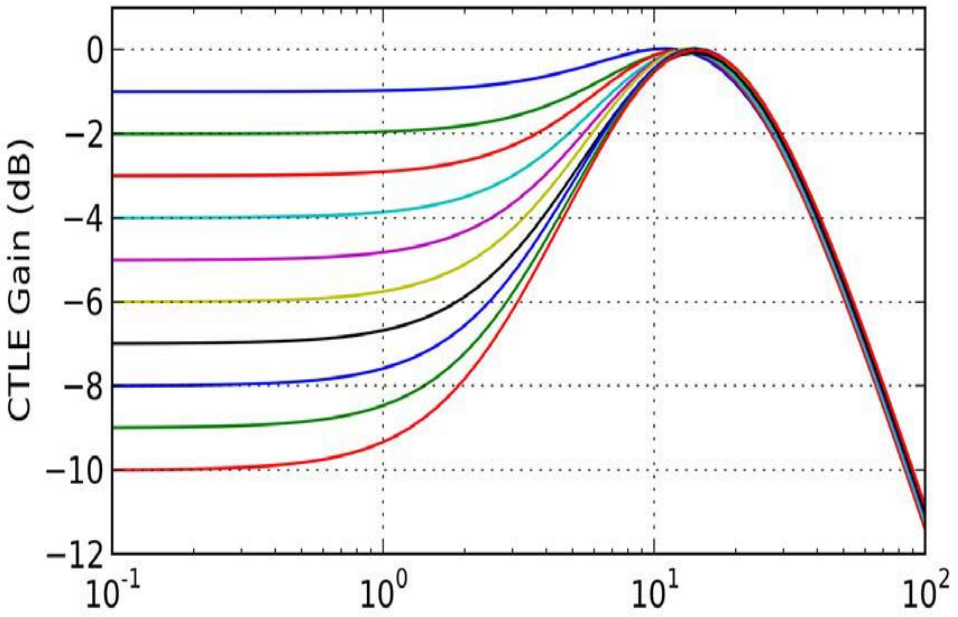
50 Gb/s PAM4 CDR Requirements

- 1st 50 Gb/s PAM4 lane Ethernet standard is for 400G (8x) and requires adaptive receiver equalization to close optical link budget and eliminate error floors [3]
- For electrical links with channel loss up to ~10dB at Nyquist/2, CTLE is sufficient [13]
- For electrical links with channel loss >10dB, DFE is required, increasing CDR power
- For optical links, 5 to 9-tap T/2-spaced FFE demonstrated to be sufficient [14]
- IEEE 802.3 is discussing the exact normative Eq. for 50G PAM4 optical links; detailed specs to be completed in 2016

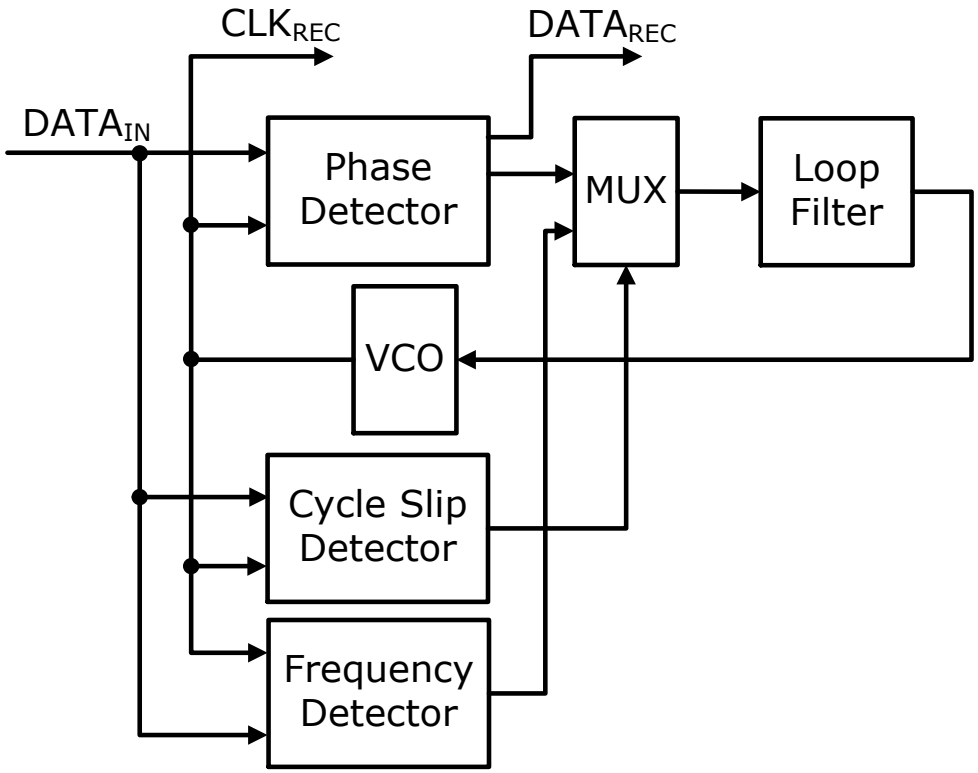
CTLE for Electrical Links

- Continuous Time Linear Equalizer (CTLE) is used to compensate for channel loss up to 10dB
- Example CTLE characteristics specified by IEEE for 25G NRZ electrical links [8]



CDR Reference-less Design

- Lowest power CDR design is reference-less by eliminating external reference clock generation circuits and internal per lane phase rotators
- Example CDR architecture

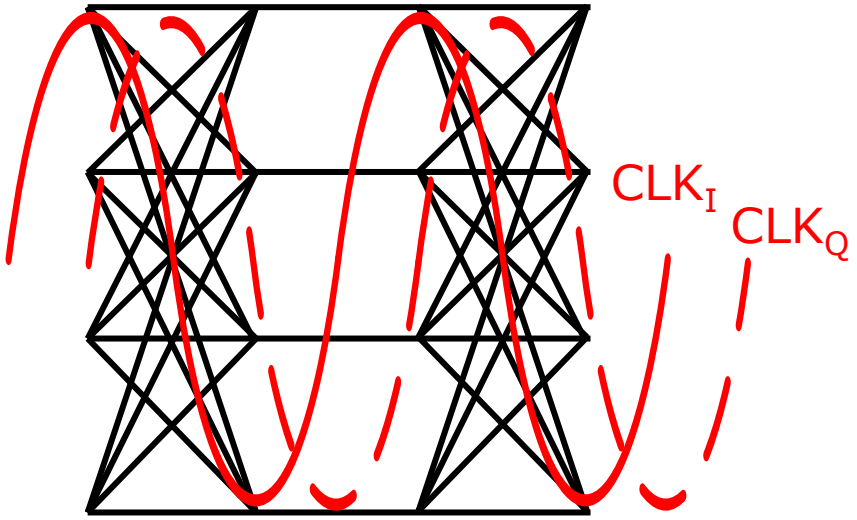


CDR Phase Detector (PD)

- Hogge phase detector [9]
  - Linear
  - T/2 wide spaced phase correction pulses
  - better jitter performance
  - higher power
- Alexander phase detector [10] [11]
  - non-linear
  - T wide spaced phase correction pulses
  - Digital in nature
  - Lower jitter performance
  - Lower power

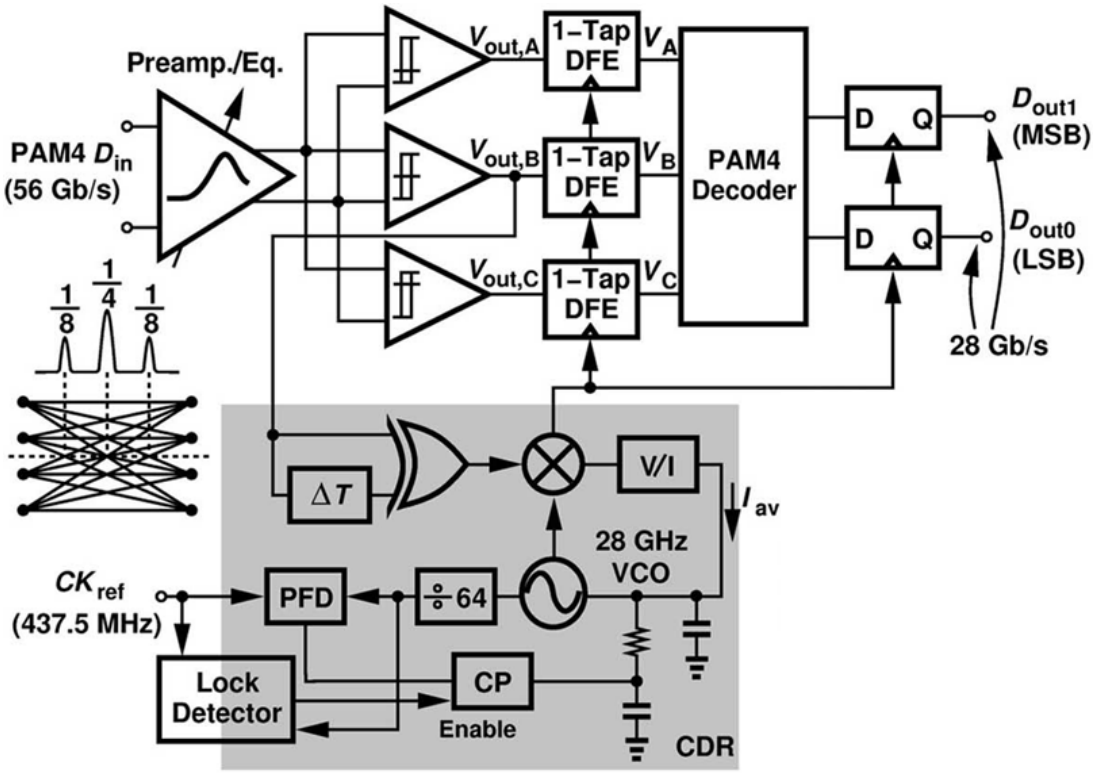
CDR Phase-Frequency Detector (PFD)

- PD has limited pull-in range requiring frequency detector to get within CDR loop bandwidth
- Preferred PFD: Pottbacker [12]
- Drawback is degradation in presence of large amount of DJ since data is used to sample in-phase and quadrature clock in 10ps window
- PAM4 eye has large amount of DJ requiring transition filtering increasing CDR power



50 Gb/s PAM4 Analog CDR Example

- 56G Gb/s PAM4 SerDes Transceiver ex. [13]
- 3 separate decision paths significantly increase PAM4 CDR circuit complexity/area/power
- Front-end linear Eq. sufficient for optical links
- DFE Eq. required for higher loss electrical links



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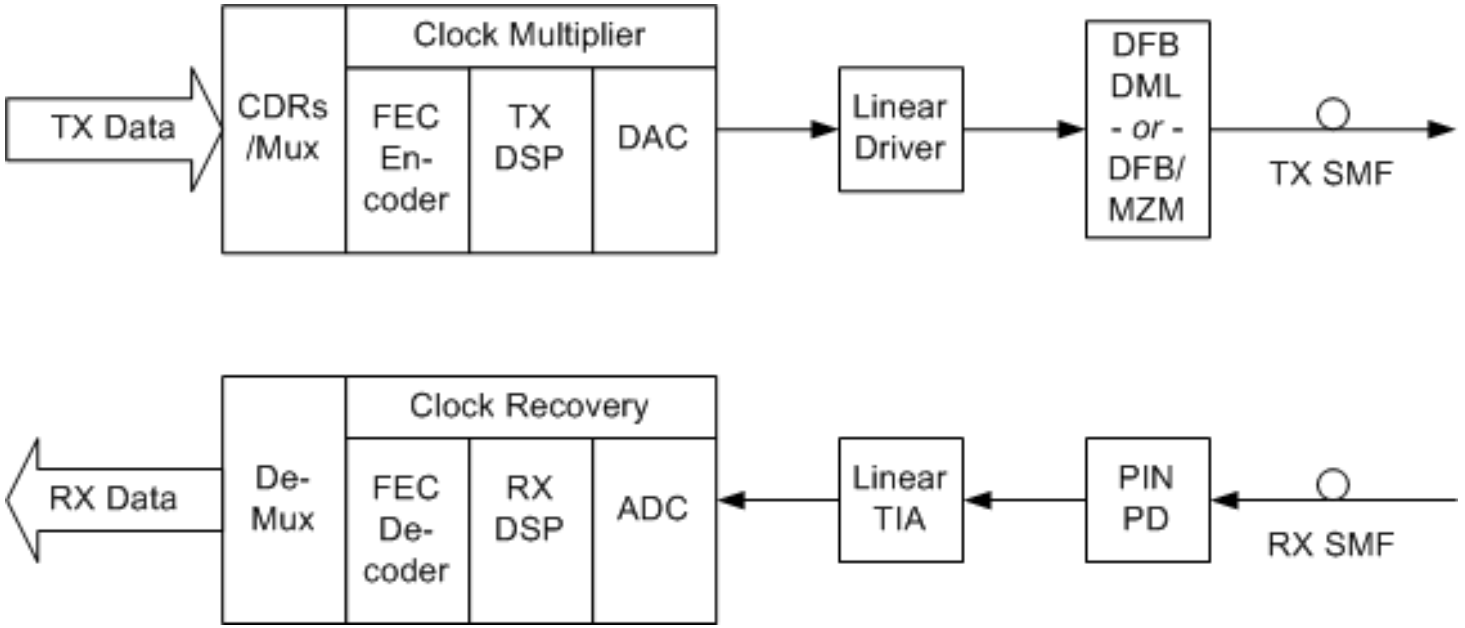
50 Gb/s PAM4 ADC/DSP CDR

- Alternative to analog CDR is digital CDR implemented in CMOS DSP with integrated ADC
- Example block diagram shows RX ADC and DSP[1] and optional TX DSP[1] and DAC[1] [1]



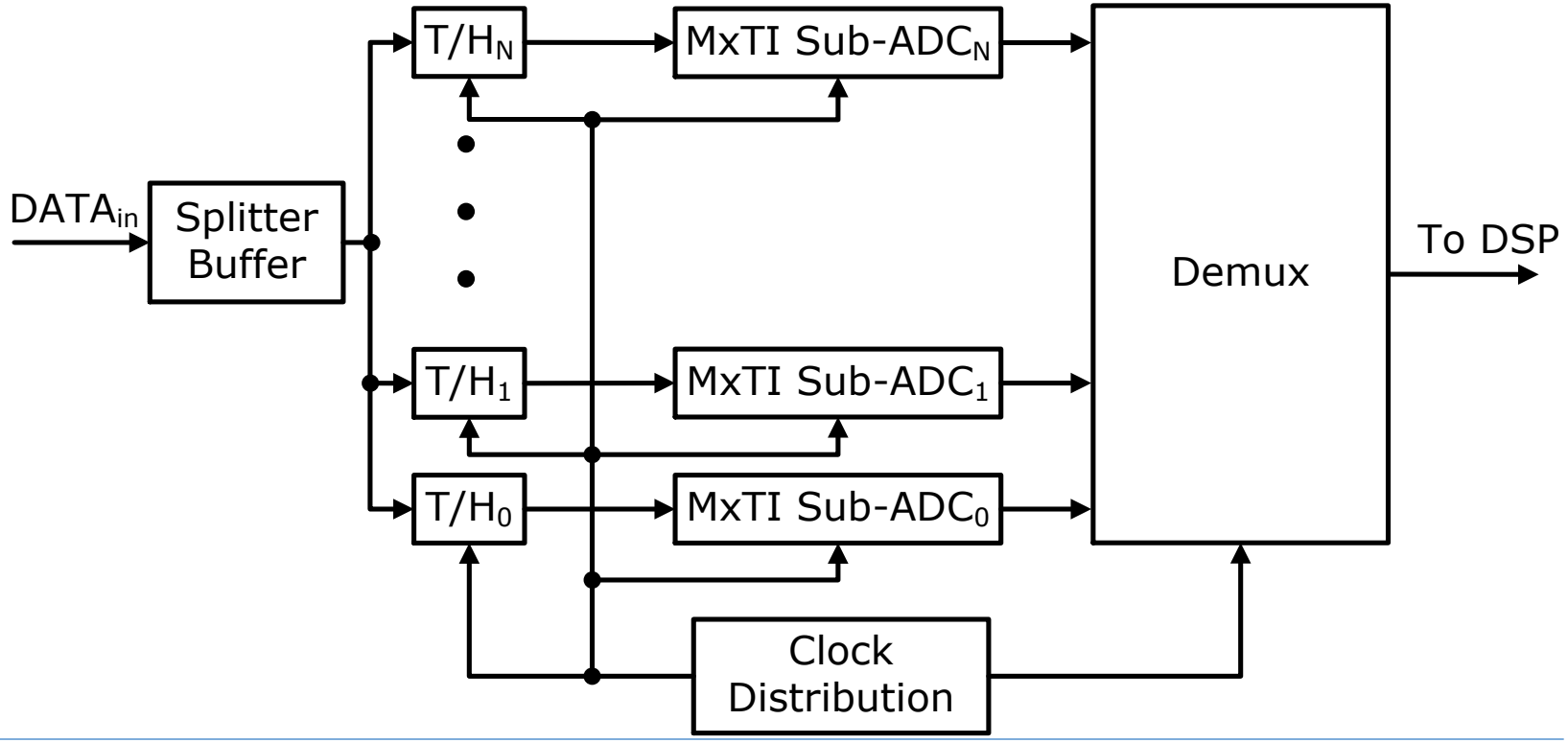
[1] Not discussed in this presentation

50 Gb/s PAM4 ADC/DSP Requirements

- Continuous-time filter for ADC anti-aliasing
- Baud-rate T-sampling ADC for lowest Eq. power
  - Requires robust timing recovery for low penalty
- High loss links require pre-equalization to enable DSP clock recovery
  - Increases latency
  - Requires low loop bandwidth
  - Reduces jitter tolerance
- DSP supports higher number of FFE and/or DFE taps beyond required for CDR to close the link, enabling minimization of optical link penalties

50 Gb/s ADC Implementation

- Time-interleaved SAR is ideal ASIC block [16]
- N master T/H (Track/Hold) x M sub-ADC T/H time-interleaved SAR ADC example:



50 Gb/s SAR ADC

- Splitter buffer determines bandwidth and THD
- Clock timing to N master T/H's and Master T/H gain-error determines resolution
- As CMOS scales, process variation and mismatch limit ADC performance improvements
- 8-bit nominal SAR ADC example [17]
  - 40nm CMOS
    - 6-bit ENOB w/ 16GHz BW
    - 63 GS/s @ 1.25W
  - 28nm CMOS
    - 6-bit ENOB w/ 25GHz BW
    - 56GS/s @ 0.8W
    - 28GS/s @ 0.4W

Summary

- 50 Gb/s PAM4 is the next high-volume short-reach interconnect lane technology
- 50 Gb/s (1x), 100 Gb/s (2x), 200 Gb/s (4x) and 400 Gb/s (8x) data rates will be supported
- 50 Gb/s PAM4 lanes requires adaptive Eq. (analog or digital) and FEC
- Circuit design challenges and opportunities
  - Linear laser driver
  - Linear trans-impedance amplifier
  - Si modulator driver and modulator
  - Multi-level adaptive clock-data recovery
  - High-speed ADC

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